**EC6302 DIGITAL ELECTRONICS L T P C 3 0 0 3**

## SUBJECT DESCRIPTION AND OBJECTIVES

SUBJECT DESCRIPTION:

Digital (electronic) circuits, represent signals by discrete bands of analog levels, rather than by a continuous range. All levels within a band represent the same signal state. Relatively small changes to the analog signal levels due to manufacturing tolerance, signal attenuation or parasitic noise do not leave the discrete envelope, and as a result are ignored by signal state sensing circuitry.

In most cases the number of these states is two, and they are represented by two voltage bands: one near a reference value (typically termed as "ground" or zero volts) and a value near the supply voltage, corresponding to the "false" ("0") and "true" ("1") values of the Boolean domain respectively.

OBJECTIVES:

- To introduce basic postulates of Boolean algebra and shows the correlation between Boolean expressions
- To introduce the methods for simplifying Boolean expressions
- To outline the formal procedures for the analysis and design of combinational circuits
- and sequential circuits
- To introduce the concept of memories and programmable logic devices.
- To illustrate the concept of synchronous and asynchronous sequential circuits

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**UNIT I MINIMIZATION TECHNIQUES AND LOGIC GATES 9**

**Minimization Techniques**: Boolean postulates and laws – De-Morgan's Theorem - Principle of Duality - Boolean expression - Minimization of Boolean expressions — Minterm – Maxterm - Sum of Products (SOP) – Product of Sums (POS) – Karnaugh map Minimization – Don't care conditions – Quine - Mc Cluskey method of minimization. **Logic Gates:** AND, OR, NOT, NAND, NOR, Exclusive–OR and Exclusive–NOR Implementations of Logic Functions using gates, NAND–NOR implementations – Multi level gate implementations- Multi output gate implementations. TTL and CMOS Logic and their characteristics – Tristate gates

**UNIT II COMBINATIONAL CIRCUITS 9**

Design procedure – Half adder – Full Adder – Half subtractor – Full subtractor – Parallel binary adder, parallel binary Subtractor – Fast Adder - Carry Look Ahead adder – Serial Adder/Subtractor - BCD adder – Binary Multiplier – Binary Divider - Multiplexer/ Demultiplexer – decoder - encoder – parity checker – parity generators – code converters - Magnitude Comparator.

**UNIT III SEQUENTIAL CIRCUITS 9**

Latches, Flip-flops - SR, JK, D, T, and Master-Slave – Characteristic table and equation – Application table – Edge triggering – Level Triggering – Realization of one flip flop using other flip flops – serial adder/subtractor- Asynchronous Ripple or serial counter – Asynchronous Up/Down counter - Synchronous counters – Synchronous Up/Down counters – Programmable counters – Design of Synchronous counters: state diagram- State table – State minimization –State assignment - Excitation table and maps-Circuit implementation - Modulo–n counter, Registers – shift registers - Universal shift registers – Shift register counters – Ring counter – Shift counters - Sequence generators

**UNIT IV MEMORY DEVICES 9**

Classification of memories – ROM - ROM organization - PROM – EPROM – EEPROM – EAPROM, RAM – RAM organization – Write operation – Read operation – Memory cycle - Timing wave forms – Memory decoding – memory expansion – Static RAM Cell- Bipolar RAM cell – MOSFET RAM cell – Dynamic RAM cell –Programmable Logic Devices – Programmable Logic Array (PLA) - Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA) - Implementation of combinational logic circuits using ROM, PLA, PAL

**UNIT V SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS 9**

**Synchronous Sequential Circuits:** General Model – Classification – Design – Use of Algorithmic State Machine – Analysis of Synchronous Sequential Circuits **Asynchronous Sequential Circuits:** Design of fundamental mode and pulse mode circuits – Incompletely specified State Machines – Problems in Asynchronous Circuits – Design of Hazard Free Switching circuits. Design of Combinational and Sequential circuits using VERILOG.

**TOTAL: 45 PERIODS**

**TEXT BOOK:**

1. M. Morris Mano, “Digital Design”, 4th Edition, Prentice Hall of India Pvt. Ltd., 2008 / Pearson Education (Singapore) Pvt. Ltd., New Delhi, 2003.

**REFERENCES:**

1. John F.Wakerly, “Digital Design”, Fourth Edition, Pearson/PHI, 2008
2. John.M Yarbrough, “Digital Logic Applications and Design”, Thomson Learning, 2006.
3. Charles H.Roth. “Fundamentals of Logic Design”, 6th Edition, Thomson Learning, 2013.
4. Donald P.Leach and Albert Paul Malvino, “Digital Principles and Applications”, 6th Edition, TMH, 2006.
5. Thomas L. Floyd, “Digital Fundamentals”, 10th Edition, Pearson Education Inc, 2011
6. Donald D.Givone, “Digital Principles and Design”, TMH, 2003.

## MICRO LESSON PLAN

| WEEKS | HOURS | LECTURE TOPIC | READING |
|---|---|---|---|
| **UNIT-I MINIMIZATION TECHNIQUES AND LOGIC GATES** | | | |
| I | 1 | **Minimization Techniques**: Boolean postulates and laws – De-Morgan's Theorem - Principle of Duality - Boolean expression | T1 |
| | 2 | Minimization of Boolean expressions–Minterm–Maxterm-Sum of Products (SOP) – Product of Sums (POS) | |
| | 3 | Karnaugh map Minimization – Don't care conditions | |
| | 4 | | |
| | 5 | Quine - Mc Cluskey method of minimization. | |
| II | 6 | **Logic Gates:** AND, OR, NOT, NAND, NOR, Exclusive–OR and Exclusive NOR Implementations of Logic Functions using gates, | |
| | 7 | NAND–NOR implementations | |
| | 8 | Multi level gate implementations- Multi output gate implementations. | |
| | 9 | TTL and CMOS Logic and their characteristics – Tristate gates | |
| **UNIT-II COMBINATIONAL CIRCUITS** | | | |
| III | 10 | Design procedure – Half adder – Full Adder | T1 |
| | 11 | Half subtractor – Full subtractor | |
| | 12 | Parallel binary adder, parallel binary Subtractor | |
| | 13 | Fast Adder- Carry Look Ahead adder – Serial Adder/Subtractor | |
| IV | 14 | BCD adder – Binary Multiplier – Binary Divider | |
| | 15 | Multiplexer/ Demultiplexer | |
| | 16 | Decoder – encoder | |
| | 17 | Parity checker – parity generators | |
| | 18 | Code converters - Magnitude Comparator. | |
| **UNIT- III SEQUENTIAL CIRCUITS** | | | |
| V | 19 | Latches, Flip-flops - SR, JK, D, T | T1 |
| | 20 | Master-Slave – Characteristic table and equation – Application table | |
| | 21 | Edge triggering – Level Triggering – Realization of one flip flop using other flip flops – serial adder/subtractor | |
| | 22 | Asynchronous Ripple or serial counter – Asynchronous Up/Down counter - | |
| | 23 | Synchronous counters – Synchronous Up/Down counters, Programmable counters , | |
| VII | 24 | Design of Synchronous counters: state diagram- State table –State minimization – | |
| | 25 | State assignment - Excitation table and maps-Circuit implementation - Modulo–n counter | |
| | 26 | Registers – shift registers - Universal shift registers – | |

| | | | |
|---|---|---|---|
| | | Shift register counters | |
| | 27 | Ring counter – Shift counters - Sequence generators. | T1 |
| **UNIT- IV MEMORY DEVICES** | | | |
| VII | 28 | Classification of memories – ROM - ROM organization - PROM – EPROM – EEPROM – EAPROM, RAM | T1 |
| | 29 | | |
| | 30 | RAM organization – Write operation – Read operation – Memory cycle - Timing wave forms – Memory decoding – memory expansion – | |
| | 31 | | |
| VIII | 32 | Static RAM Cell- Bipolar RAM cell – MOSFET RAM cell – Dynamic RAM cell | |
| | 33 | | |
| | 34 | Programmable Logic Devices – Programmable Logic Array (PLA) - Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA) | |
| | 35 | | |
| | 36 | Implementation of combinational logic circuits using ROM, PLA, PAL | |
| **UNIT V- SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS** | | | |
| IX | 37 | **Synchronous Sequential Circuits:** General Model – Classification – Design – Use of Algorithmic State Machine | T1 |
| | 38 | Analysis of Synchronous Sequential Circuits | |
| | 39 | **Asynchronous Sequential Circuits:** Design of fundamental mode circuits | |
| | 40 | Design of pulse mode circuits | |
| X | 41 | Incompletely specified State Machines | |
| | 42 | Problems in Asynchronous Circuits – Design of Hazard Free Switching circuits. | |
| | 43 | | |
| | 44 | Design of Combinational circuits using VERILOG. | |
| | 45 | Design of Sequential circuits using VERILOG. | |

**Prepared by:**

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