SARDAR RAJA COLLEGE OF ENGINEERING, ALANGULAM

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MICRO LESSON PLAN

SUBJECT : VLSI DESIGN

SUBJECT CODE : EC2354

CLASS : III Year / VI SEM

STAFF: Ms.T.THANYA, AP/ECE

EC2354 VLSI DESIGN L T P C
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UNIT I CMOS TECHNOLOGY 9

A brief History-MOS transistor, Ideal I-V characteristics, C-V characteristics, Non ideal IV effects, DC transfer characteristics - CMOS technologies, Layout design Rules, CMOS process enhancements, Technology related CAD issues, Manufacturing issues.

UNIT II CIRCUIT CHARACTERIZATION AND SIMULATION 9

Delay estimation, Logical effort and Transistor sizing, Power dissipation, Interconnect, Design margin, Reliability, Scaling- SPICE tutorial, Device models, Device characterization, Circuit characterization, Interconnect simulation

UNIT III COMBINATIONAL AND SEQUENTIAL CIRCUIT DESIGN 9

Circuit families –Low power logic design – comparison of circuit families – Sequencing static circuits, circuit design of latches and flip flops, Static sequencing element methodology- sequencing dynamic circuits – synchronizers

UNIT IV CMOS TESTING 9

Need for testing- Testers, Text fixtures and test programs- Logic verification- Silicon debug principles- Manufacturing test – Design for testability – Boundary scan

UNIT V SPECIFICATION USING VERILOG HDL 9

Basic concepts- identifiers- gate primitives, gate delays, operators, timing controls, procedural assignments conditional statements, Data flow and RTL, structural gate level switch level modeling, Design hierarchies, Behavioral and RTL modeling, Test benches, Structural gate level description of decoder, equality detector, comparator, priority encoder, half adder, full adder, Ripple carry adder, D latch and D flip flop.

TOTAL: 45 PERIODS

TEXT BOOK:

1. Weste and Harris: CMOS VLSI DESIGN (Third edition) Pearson Education, 2005.

2. Uyemura J.P: Introduction to VLSI circuits and systems, Wiley 2002.

REFERENCES:

1 D.A.Pucknell & K.Eshraghian Basic VLSI Design, Third edition, PHI, 2003

2 Wayne Wolf, Modern VLSI design, Pearson Education, 2003

3 M.J.S.Smith: Application specific integrated circuits, Pearson Education, 1997

4 J.Bhasker, "Verilog HDL Primer", BS publication, 2001

5 Ciletti Advanced Digital Design with the Verilog HDL, Prentice Hall of India, 2003

SUBJECT DESCRIPTION AND OBJECTIVES

DESCRIPTION

This subject is designed to provide necessary design and analysis skills needed to contribute effectively as VLSI circuit designer. Device level issues for MOSFETs, e.g. V-I characteristics, threshold voltage, etc. analyzed to provide insights into their effects on circuit design.

Basic gates, CMOS inverter, pass transistors and transmission gates will be thoroughly understood. Effects of device sizing and various circuits parasitic will be studied on design metrics like, speed, power and area will be analyzed. Students will acquire circuit design skills, understand transistor sizing and wire design issues related to digital CMOS circuits.

Design and analysis of various static and dynamic, combinational and sequential CMOS circuit styles will be introduced. Advantages and disadvantages of different design styles will be understood. After understanding basic circuit design issues students will delve into subsystem design of adders, multipliers, memory. Clocking and timing issues will be understood.

Lastly, students will be introduced to the concept of technology scaling and its effect on circuit performance. This subject also involves the use of VLSI CAD tools to layout, check and simulates small circuits in homework assignments and a final full-custom design project.

OBJECTIVES:

- To learn the basic CMOS circuits.
- To learn the CMOS process technology.
- To learn techniques of chip design using programmable devices.
- To learn the concepts of designing VLSI subsystems.
- To learn the concepts of modeling a digital system using Hardware Description Language.

MICRO LESSON PLAN

Hours	LECTURE TOPICS	READING
UNIT I : CMOS TECHNOLOGY		
1	Introduction, A brief History-MOS transistor	T1
2	Ideal I-V characteristics	T1
3	C-V characteristics	T1
4	Non ideal I-V effects	T1
5	DC transfer characteristics	T1
6	CMOS technologies	T1
7	Layout design Rules (A/ V)	T1
8,9	CMOS process enhancements (A/ V)	T1
10	Technology related CAD issues, Manufacturing issues	T1
UNIT II : CIRCUIT CHARACTERIZATION AND SIMULATION		
11	Delay estimation	T1
12	Logical effort and Transistor sizing	T1
13	Power dissipation	T1
14	Interconnect	T1
15	Design margin	T1
16	Reliability	T1
17	Scaling	T1
18	SPICE tutorial (A/V)	T1
19	Device models	T1
20,21	Device characterization	T1
22	Circuit characterization	T1
23	Interconnect simulation	T1
UNIT III : COMBINATIONAL AND SEQUENTIAL CIRCUIT DESIGN		
24,25	Circuit families	T1
26	Low power logic design	T1
27	Comparison of circuit families	T1
28,29	Sequencing static circuits	T1
30	circuit design of latches and flip flops (A/V)	T1
31	Static sequencing element methodology	T1
32	Sequencing dynamic circuits	T1
33	synchronizers	T1

UNIT IV : CMOS TESTING		
34,35	Need for testing	T1
36	Testers, Text fixtures and test programs	T1
37	Logic verification	T1
38	Silicon debug principles	T1
39	Manufacturing test	T1
40	Design for testability	T1
41,42	Boundary scan (A/V)	T1
UNIT V : SPECIFICATION USING VERILOG HDL		
43	Basic concepts- identifiers- gate primitives	R4
44	gate delays, operators, timing controls	R4
45	procedural assignments conditional statements	R4
46	Data flow and RTL, structural gate level switch level modeling	R4
47	Design hierarchies, Behavioral and RTL modeling	R4
48	Test benches, Structural gate level description of decoder	R4
49	equality detector, comparator, priority encoder	R4
50	half adder, full adder, Ripple carry adder	R4
51	D latch and D flip flop	R4

T1. Weste and Harris: CMOS VLSI DESIGN (Third edition) Pearson Education, 2005.

R4. J.Bhasker, “Verilog HDL Primer”, BS publication, 2001.