SARDAR RAJA COLLEGE OF ENGINEERING, ALANGULAM

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MICRO LESSON PLAN

SUBJECT NAME /CODE : COMPUTER ARCHITECTURE & ORGANIZATION

SUBJECT CODE : EC 2303

CLASS : III Year ECE / V SEM

STAFF: Ms. S. SUDHA, Asst. Prof,

DEPT. OF ECE

EC2303 COMPUTER ARCHITECTURE AND ORGANIZATION L T P C 3 0 0 3

UNIT I INTRODUCTION 9

Computing and Computers, Evolution of Computers, VLSI Era, System Design- Register

Level, Processor Level, CPU Organization, Data Representation, Fixed – Point Numbers, Floating Point Numbers, Instruction Formats, Instruction Types. Addressing modes.

UNIT II DATA PATH DESIGN 9

Fixed Point Arithmetic, Addition, Subtraction, Multiplication and Division, Combinational and Sequential ALUs, Carry look ahead adder, Robertson algorithm, booth's algorithm, non-restoring division algorithm, Floating Point Arithmetic, Coprocessor, Pipeline Processing, Pipeline Design, Modified booth's Algorithm

UNIT III CONTROL DESIGN 9

Hardwired Control, Microprogrammed Control, Multiplier Control Unit, CPU Control Unit, Pipeline Control, Instruction Pipelines, Pipeline Performance, Superscalar Processing, Nano Programming.

UNIT IV MEMORY ORGANIZATION 9

Random Access Memories, Serial - Access Memories, RAM Interfaces, Magnetic Surface Recording, Optical Memories, multilevel memories, Cache & Virtual Memory, Memory Allocation, Associative Memory.

UNIT V SYSTEM ORGANIZATION 9

Communication methods, Buses, Bus Control, Bus Interfacing, Bus arbitration, IO and system control, IO interface circuits, Handshaking, DMA and interrupts, vectored interrupts, PCI interrupts, pipeline interrupts, IOP organization, operation systems, multiprocessors, fault tolerance, RISC and CISC processors, Superscalar and vector processor.

TOTAL= 45 PERIODS

TEXTBOOKS

1. John P.Hayes, 'Computer architecture and Organisation', Tata McGraw-Hill, Third edition, 1998.

2. V.Carl Hamacher, Zvonko G. Varanesic and Safat G. Zaky, "Computer Organisation", V edition, McGraw-Hill Inc, 1996.

REFERENCES

1. Morris Mano, "Computer System Architecture", Prentice-Hall of India, 2000.

2. Paraami, "Computer Architecture", BEH R002, Oxford Press.

3. P.Pal Chaudhuri, , "Computer organization and design", 2nd Ed., Prentice Hall of India, 2007.

4. G.Kane & J.Heinrich, ' MIPS RISC Architecture ', Englewood cliffs, New Jersey, Prentice Hall, 1992.

SUBJECT DESCRIPTION AND OBJECTIVES

OBJECTIVES:

- To have a thorough understanding of the basic structure and operation of a digital computer.
- To discuss in detail the operation of the arithmetic unit including the algorithms implementation of fixed-point and floating-point addition, subtraction, multiplication division.
- To study in detail the different types of control and the concept of pipelining.
- To study the hierarchical memory system including cache memories and virtual memory.
- To study the different ways of communicating with I/O devices and standard I/O interfaces.

DESCRIPTION :

In electronics engineering and computer engineering, computer architecture is a set of disciplines that describes a computer system by specifying its parts and their relations.

For example, at a high level, computer architecture may be concerned with how the central processing unit (CPU) acts and how it uses computer memory. Some fashionable (2011) computer architectures include cluster computing and non-uniform memory access.

Computer architects use computers to design new computers. Emulation software can run programs written in a proposed instruction set. While the design is very easy to change at this stage, compiler designers often collaborate with the architects, suggesting improvements in the instruction set. Modern emulators may measure time in clock cycles: estimate energy consumption in joules, and give realistic estimates of code size in bytes. These affect the convenience of the user, the life of a battery, and the size and expense of the computer's largest physical part: its memory. That is, they help to estimate the value of a computer design.

MICRO LESSON PLAN

WEEK	HOURS	LECTURE TOPICS	BOOK
	UNIT I INTRODUCTION		
I	1.	Computing and Computers (AV Class)	T1
	2.	Evolution of Computers, VLSI Era (AV Class)	
	3.	System Design- Register Level, Processor Level	
	4.	CPU Organization	
	5.	Data Representation, Fixed – Point Numbers	
II	6.	Floating Point Numbers	
	7.	Instruction Formats	
	8.	Instruction Types	
	9.	Addressing modes	
	UNIT II DATA PATH DESIGN		
III	10.	Fixed Point Arithmetic, Addition, Subtraction, Multiplication and Division	T1
	11.	Combinational and Sequential ALUs	
	12.	Carry look ahead adder (AV Class)	
	13.	Robertson algorithm	
	14.	Booth's algorithm	
IV	15.	Non-restoring division algorithm	
	16.	Floating Point Arithmetic Coprocessor	
	17.	Pipeline Processing, Pipeline Design (AV Class)	
	18.	modified Booth's Algorithm	
	UNIT III CONTROL DESIGN		
V	19	Hardwired Control	T1
	20	Micro programmed Control	
	21	Multiplier Control Unit	
	22	CPU Control Unit	
	23	Pipeline Control	
VI	24	Instruction Pipelines	
	25	Pipeline Performance (AV Class)	
	26	Superscalar Processing (AV Class)	
	27	Nano Programming	
	UNIT IV MEMORY ORGANIZATION		
VII	28	Random Access Memories	T1
	29	Serial - Access Memories	
	30	RAM Interfaces (AV Class)	
	31	Magnetic Surface Recording	
	32	Optical Memories	
VIII	33	multilevel memories	
	34	Cache & Virtual Memory (AV Class)	
	35	Memory Allocation	
	36	Associative Memory	

UNIT V SYSTEM ORGANIZATION			
IX	37	Communication methods, Buses, Bus Control (AV Class)	T1&T2
	38	Bus Interfacing, Bus arbitration	
	39	IO and system control, IO interface circuits	
	40	Handshaking, DMA and interrupts	
	41	Vectored interrupts, PCI interrupts,Pipeline interrupts	
X	42	IOP organization, operation systems	
	43	Multiprocessors, fault tolerance	
	44	RISC and CISC processors (AV Class)	
	45	Superscalar and vector processor	

STAFF: Ms. S. SUDHA, Asst. Prof,

DEPT. OF ECE